Translation

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Form PCT/IPEA/416
03/039 WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CH2004/000388	24.06.2004	23.07.2003
International Patent Classification (IPC) or national classification and IPC		
H02M7/48		
Applicant		
ABB SCHWEIZ AG		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 19 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *(sent to the applicant and to the International Bureau)* a total of 5 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s))

      _____, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).
4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
Name and mailing address of the IPEA/EP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/CH2004/000388

Box No. I Basis of the report

1. With regard to the language, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This report is based on translations from the original language into the following language _____, which is the language of a translation furnished for the purposes of:

☐ international search (Rule 12.3 and 23.1(b))

☐ publication of the international application (Rule 12.4)

☐ international preliminary examination (Rule 55.2 and/or 55.3)

2. With regard to the elements of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

☐ the international application as originally filed/furnished

☒ the description:

pages 1-17 as originally filed/furnished

pages* _____ received by this Authority on _____

pages* _____ received by this Authority on _____

☒ the claims:

nos. _____ as originally filed/furnished

nos.* _____ as amended (together with any statement) under Article 19

nos.* 1-8 received by this Authority on 19.09.2005 with telefax

nos.* _____ received by this Authority on _____

☒ the drawings:

sheets 1/10-10/10 as originally filed/furnished

sheets* _____ received by this Authority on _____

sheets* _____ received by this Authority on _____

☐ a sequence listing and/or any related table(s) – see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, nos. _____

☐ the drawings, sheets/figs _____

☐ the sequence listing *(specify)*: _____

☐ any table(s) related to sequence listing *(specify)*: _____

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

☐ the description, pages _____

☐ the claims, nos. _____

☐ the drawings, sheets/figs _____

☐ the sequence listing *(specify)*: _____

☐ any table(s) related to sequence listing *(specify)*: _____

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/CH2004/000388

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-8	YES
	Claims		NO
Inventive step (IS)	Claims	1-8	YES
	Claims		NO
Industrial applicability (IA)	Claims	1-8	YES
	Claims		NO

2. Citations and explanations (Rule 70.7)

1. This report makes reference to the following document:

D1: WO 03/017457 A (ROJAS ROMERO MANUEL ROBERTO; EMERSON ENERGY SYSTEMS AB (SE)) 27 February 2003 (2003-02-27)

2. Novelty and inventive step

2.1 Claim 1

Claim 1 is interpreted according to the statements in Box VIII.

D1 is considered to be the prior art closest to the subject matter of claim 1.

D1 discloses, in the wording of claim 1 (to the extent possible); the references in parentheses are to D1:

converter circuit for a plurality of phases (*figure 2: phases A, B, C*), said circuit having a first switching group system provided for each phase (*figure 2: first*

switching group system for phase A comprises diodes D13 and D14 connected at point R, the switches included in the controllable power semiconductor switch S1 and shown in figure 3a in conjunction with page 6, lines 10-13, capacitor C12 and part of the capacitance of capacitor C2; first switching group system for phase B comprises diodes D23 and D24 connected at point S, the switches included in the controllable power semiconductor switch S2 and shown in figure 3a in conjunction with page 6, lines 10-13, capacitor C22 and part of the capacitance of capacitor C2; first switching group system for phase C comprises diodes D33 and D34 connected at point T, the switches included in the controllable power semiconductor switch S3 and shown in figure 3a in conjunction with page 6, lines 10-13, capacitor C32 and part of the capacitance of capacitor C2) and having an additional or n additional switching group systems provided for each phase, wherein n > 1 (*figure 2: additional switching group system for phase A: system consisting of diode D11, capacitor C11, diode D16 and capacitor C14; additional switching group system for phase B: system consisting of diode D21, capacitor C21, diode D26 and capacitor C24; additional switching group system for phase C: system consisting of diode D31, capacitor C31, diode D36 and capacitor C34*),

said switching group system(s) (each) having a first main switching group (*figure 2: first main switching group for phase A consists of diode 13 and capacitor C12; first main switching group for phase B consists of diode 23 and capacitor C22; first main switching group for phase C consists of diode 33 and capacitor C32*) made up of a power semiconductor switch (*figure 2: power semiconductor*

switch for phase A: diode D13; power semiconductor switch for phase B: diode D23; power semiconductor switch for phase C: diode D33) and a separate capacitor connected to the power semiconductor switch (*figure 2: for phase A: separate capacitor C12 is connected to diode 23; for phase C: separate capacitor C32 is connected to diode 33*); the power semiconductor switch of the first main switching group being made up exclusively of a passive, non-controllable electronic component with unidirectional current flow (*figure 2: for phase A: diode D13, for phase B: diode D23, for phase C: diode D33*),

said switching group system(s) (each) having at least one intermediate switching group made up of two controllable power semiconductor switches connected in series (*figures 2 and 3a in conjunction with page 6, lines 10-13: for phase A, the controllable power semiconductor switch within S1; for phase B, the controllable power semiconductor switch within S2; for phase C, the controllable power semiconductor switch within S3*) and a separate capacitor, the or one of the intermediate switching groups being connected to the first main switching group (*figure 2: for phase A: the connection at point R; for phase B: the connection at point S; for phase C: the connection at point T*),

and said switching group system(s) (each) having a second main switching group made up of a power semiconductor switch, the power semiconductor switch of the second main switching group (*figure 2: for phase A, the power semiconductor switch and thus the second main switching group consists of diode D14; for phase B, the power semiconductor switch and thus the second main switching group consists of diode D24; for phase C, the power*

semiconductor switch and thus the second main switching group consists of diode D34) being made up exclusively of a passive, non-controllable electronic component with unidirectional current flow (*figure 2: for phase A: diode D14; for phase B: diode D24; for phase C: diode D34*) and the or one of the intermediate switching groups being connected to the second main switching group (*figure 2: for phase A: connection of diode 14 to point R and thus connection to the aforementioned intermediate switching group; for phase B: connection of diode 24 to point S and thus connection to the aforementioned intermediate switching group; for phase C: connection of diode 34 to point T and thus connection to the aforementioned intermediate switching group*),

wherein,

in the additional or each of the n additional switching group systems, the intermediate switching group (*figure 2: for phase A: the adjacent intermediate switching group comprises capacitor C11; for phase B: the adjacent intermediate switching group comprises capacitor C21; for phase C: the adjacent intermediate switching group comprises capacitor C31*) adjacent to the first main switching group (*figure 2: for phase A: the first main switching group comprises diode D11; for phase B: the first main switching group comprises diode D21; for phase C: the first main switching group comprises diode D31*) is connected in series to the first main switching group (*figure 2: for phase A, capacitor C11 of the adjacent intermediate switching group is connected in series to diode D11 of the first main switching group; for phase B, capacitor C21 of the adjacent intermediate switching group is connected in series to diode D21 of the first*

main switching group; for phase C, capacitor C31 of the adjacent intermediate switching group is connected in series to diode D31 of the first main switching group) and the intermediate switching group (*figure 2: for phase A: the adjacent intermediate switching group comprises capacitor C14; for phase B: the adjacent intermediate switching group comprises capacitor C24; for phase C: the adjacent intermediate switching group comprises capacitor C34*) adjacent to the second main switching group (*figure 2: for phase A: the second main switching group comprises diode D16; for phase B: the second main switching group comprises diode D26; for phase C: the second main switching group comprises diode D36*) is connected in series to the second main switching group (*figure 2: for phase A, capacitor C14 of the adjacent intermediate switching group is connected in series to diode D16 of the second main switching group; for phase B, capacitor C24 of the adjacent intermediate switching group is connected in series to diode D26 of the second main switching group; for phase C, capacitor C34 of the adjacent intermediate switching group is connected in series to diode D36 of the second main switching group*),

wherein the first main switching group of the first switching group system and the first main switching groups of the additional or n additional switching group systems are connected to each other in series (*figure 2: for phase A, the series connection is made via diode D12; for phase B, the series connection is made via diode 22; for phase C, the series connection is made via diode 32*),

wherein the second main switching group of the first

switching group system and the second main switching groups of the additional or n additional switching group systems are connected to each other in series (*figure 2: for phase A, the series connection is made via diode 15; for phase B, the series connection is made via diode 25; for phase C, the series connection is made via diode 35*), and

wherein, with a plurality of phases, the additional switching group systems or the n additional switching group systems of the phases are connected to each other in parallel (*figure 2: the additional switching group systems of the phases are connected to each other in parallel via points P and N*),

wherein, in the first switching group system and in the additional or in each of the n additional switching group systems, one of the controllable power semiconductor switches of an intermediate switching group is connected to the capacitor of the same intermediate switching group,

wherein, in the first switching group system, the intermediate switching group adjacent to the first main switching group is connected in parallel to the first main switching group (*figure 2: for phase R: the parallel connection is made at point R; for phase S: the parallel connection is made at point S; for phase T: the parallel connection is made at point T*), and

wherein, in the first switching group system, the intermediate switching group adjacent to the second main switching group is connected in parallel to the second main switching group (*figure 2: for phase R: the parallel connection is made at point R; for phase S: the parallel connection is made at point S; for phase T: the parallel*

connection is made at point T).

The subject matter of claim 1 differs from the known document D1 in that

(a) each intermediate group of each switching group system has a separate capacitor;

(b) in the first switching group system and in the additional or in each of the n additional switching group systems, one of the controllable power semiconductor switches of each intermediate switching group is connected to the capacitor of the same intermediate switching group;

It is clear from the combination of distinguishing features in point (b) that controllable power semiconductor switches must also be present in the additional or n additional switching group systems. This combination of features is not disclosed in either D1, figure 2, or the remaining available prior art, and therefore does not appear to be obvious.

Claim 1 is therefore novel and appears to be inventive (PCT Article 33(1) to (3)).

2.2 Claim 2

Claim 2 is interpreted according to the statements in Box VIII.

D1 is considered to be the prior art closest to the

subject matter of claim 2.

D1 discloses, in the wording of claim 2 (to the extent possible); the references in parentheses are to D1:

converter circuit for a plurality of phases (*figure 2: phases A, B, C*), said circuit having a first switching group system provided for each phase (*figure 2: first switching group system for phase A comprises diodes D13 and D14 connected at point R, the switches included in the controllable power semiconductor switch S1 and shown in figure 3a in conjunction with page 6, lines 10-13, capacitor C12 and part of the capacitance of capacitor C2; first switching group system for phase B comprises diodes D23 and D24 connected at point S, the switches included in the controllable power semiconductor switch S2 and shown in figure 3a in conjunction with page 6, lines 10-13, capacitor C22 and part of the capacitance of capacitor C2; first switching group system for phase C comprises diodes D33 and D34 connected at point T, the switches included in the controllable power semiconductor switch S3 and shown in figure 3a in conjunction with page 6, lines 10-13, capacitor C32 and part of the capacitance of capacitor C2*) and having an additional or n additional switching group systems provided for each phase, wherein n > 1 (*figure 2: additional switching group system for phase A: system consisting of diode D11, capacitor C11, diode D16 and capacitor C14; additional switching group system for phase B: system consisting of diode D21, capacitor C21, diode D26 and capacitor C24; additional switching group system for phase C: system consisting of diode D31, capacitor C31, diode D36 and capacitor*

C34),

said switching group system(s) (each) having a first main switching group (*figure 2: first main switching group for phase A consists of diode 13 and capacitor C12; first main switching group for phase B consists of diode 23 and capacitor C22; first main switching group for phase C consists of diode 33 and capacitor C32*) made up of a power semiconductor switch (*figure 2: power semiconductor switch for phase A: diode D13; power semiconductor switch for phase B: diode D23; power semiconductor switch for phase C: diode D33*) and a separate capacitor connected to the power semiconductor switch (*figure 2: for phase A: separate capacitor C12 is connected to diode 23; for phase C: separate capacitor C32 is connected to diode 33*); the power semiconductor switch of the first main switching group being made up exclusively of a passive, non-controllable electronic component with unidirectional current flow (*figure 2: for phase A: diode D13, for phase B: diode D23, for phase C: diode D33*),
said switching group system(s) (each) having at least one intermediate switching group made up of two controllable power semiconductor switches connected in series (*figures 2 and 3a in conjunction with page 6, lines 10-13: for phase A, the controllable power semiconductor switch within S1; for phase B, the controllable power semiconductor switch within S2; for phase C, the controllable power semiconductor switch within S3*) and a separate capacitor, the or one of the intermediate switching groups being connected to the first main switching group (*figure 2: for phase A: the connection at point R; for phase B: the connection at point S; for*

phase C: the connection at point T),
and said switching group system(s) (each) having a second main switching group made up of a power semiconductor switch, the power semiconductor switch of the second main switching group (*figure 2: for phase A, the power semiconductor switch and thus the second main switching group consists of diode D14; for phase B, the power semiconductor switch and thus the second main switching group consists of diode D24; for phase C, the power semiconductor switch and thus the second main switching group consists of diode D34*) being made up exclusively of a passive, non-controllable electronic component with unidirectional current flow (*figure 2: for phase A: diode D14; for phase B: diode D24; for phase C: diode D34*) and the or one of the intermediate switching groups being connected to the second main switching group (*figure 2: for phase A: connection of diode 14 to point R and thus connection to the aforementioned intermediate switching group; for phase B: connection of diode 24 to point S and thus connection to the aforementioned intermediate switching group; for phase C: connection of diode 34 to point T and thus connection to the aforementioned intermediate switching group*),
wherein,
in the additional or each of the n additional switching group systems, the intermediate switching group (*figure 2: for phase A: the adjacent intermediate switching group comprises capacitor C11; for phase B: the adjacent intermediate switching group comprises capacitor C21; for phase C: the adjacent intermediate switching group comprises capacitor C31*) adjacent to the first main switching group (*figure 2: for phase A: the first main*

switching group comprises diode D11; for phase B: the first main switching group comprises diode D21; for phase C: the first main switching group comprises diode D31) is connected in series to the first main switching group (*figure 2: for phase A, capacitor C11 of the adjacent intermediate switching group is connected in series to diode D11 of the first main switching group; for phase B, capacitor C21 of the adjacent intermediate switching group is connected in series to diode D21 of the first main switching group; for phase C, capacitor C31 of the adjacent intermediate switching group is connected in series to diode D31 of the first main switching group*) and the intermediate switching group (*figure 2: for phase A: the adjacent intermediate switching group comprises capacitor C14; for phase B: the adjacent intermediate switching group comprises capacitor C24; for phase C: the adjacent intermediate switching group comprises capacitor C34*) adjacent to the second main switching group (*figure 2: for phase A: the second main switching group comprises diode D16; for phase B: the second main switching group comprises diode D26; for phase C: the second main switching group comprises diode D36*) is connected in series to the second main switching group (*figure 2: for phase A, capacitor C14 of the adjacent intermediate switching group is connected in series to diode D16 of the second main switching group; for phase B, capacitor C24 of the adjacent intermediate switching group is connected in series to diode D26 of the second main switching group; for phase C, capacitor C34 of the adjacent intermediate switching group is connected in series to diode D36 of the second main switching group*),

wherein the first main switching group of the first switching group system and the first main switching groups of the additional or n additional switching group systems are connected to each other in series (*figure 2: for phase A, the series connection is made via diode D12; for phase B, the series connection is made via diode 22; for phase C, the series connection is made via diode 32*),

wherein the second main switching group of the first switching group system and the second main switching groups of the additional or n additional switching group systems are connected to each other in series (*figure 2: for phase A, the series connection is made via diode 15; for phase B, the series connection is made via diode 25; for phase C, the series connection is made via diode 35*), and

wherein, with a plurality of phases, the additional switching group systems or the n additional switching group systems of the phases are connected to each other in parallel (*figure 2: the additional switching group systems of the phases are connected to each other in parallel via points P and N*),

wherein, in the first switching group system and in the additional or in each of the n additional switching group systems, the power semiconductor switch of the first main switching group has an additional passive, non-controllable electronic component with unidirectional current flow, the additional electronic component being connected in series to the existing electronic component (*figure 2: diodes D15, D25 and D35 can be regarded as power switches and as connected in series to the existing*

components D14, D24 and D34, which are regarded as existing electronic components of the second main switching group in the first switching group system),
wherein, in the first switching group system, the connecting point for the two controllable power semiconductor switches of each intermediate switching group is connected to the capacitor of the same intermediate switching group,
wherein, in the first switching group system, the intermediate switching group adjacent to the first main switching group is connected to the connecting point for the two electronic components of the first main switching group via one of the two controllable power semiconductor switches (*figure 2: the connection between connecting points F1, F2, F3 and switches S1, S2 and S3 is made via diodes D13, D23 and D33*), and
wherein, in the first switching group system, the intermediate switching group adjacent to the second main switching group is connected to the connecting point for the two electronic components of the second main switching group via the other controllable power semiconductor switch (*figure 2: the connection between connecting points G1, G2, G3 and switches S1, S2 and S3 is made via diodes D14, D24 and D34*).

The subject matter of claim 2 differs from the known document D1 in that

(a) each intermediate group of each switching group system has a separate capacitor;

(b) in the additional or in each of the n additional

switching group systems, the power semiconductor switch of the first main switching group has an additional passive, non-controllable electronic component with unidirectional current flow, the additional electronic component being connected in series to the existing electronic component;

(c) in the additional or in each of the n additional switching group systems, the power semiconductor switch of the second main switching group has an additional passive, non-controllable electronic component with unidirectional current flow, the additional electronic component being connected in series to the existing electronic component;

(d) in the first switching group system, the connecting point for the two controllable power semiconductor switches of each intermediate switching group is connected to the capacitor of the same intermediate switching group.

It is clear from the combination of distinguishing features in point (d) that the connecting point for the two controllable power semiconductor switches of each intermediate switching group is connected to the capacitor of the same intermediate switching group. This combination of features is not disclosed in D1, figure 2, and does not appear to be obvious from the remaining available prior art.

Claim 2 is therefore novel and appears to be inventive (PCT Article 33(1) to (3)).

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

2.3 Claims 3 to 8

Claims 3 to 8 are dependent on claims 1 and 2 and therefore also meet the PCT requirements for novelty and inventive step.

3. Industrial applicability

No objections are raised with regard to the industrial applicability of the subject matter defined in claims 1 to 8 (PCT Article 33(1) and (4)).

Box No. VIII **Certain observations on the international application**

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

The phrase "said switching group system (1, 10.1, ..., 10.n) used three times in claims 1 and 2 is not clear (PCT Article 6). The use of this noun in the singular implies that there is only one switching group system. However, both claim 1 and claim 2 refer to a "first switching group system (1)" and at least one "additional switching group system" for each phase. The converter circuit for a plurality of phases in both claim 1 and claim 2 must therefore have at least two switching group systems per phase.

An addition, the description, page 12, line 10 ff., and the figures included with the international application suggest that the combination of features following each instance of the phrase "said switching group system (1, 10.1, ..., 10.n)" both in the preamble of claim 1 and in the preamble of claim 2 must refer to each "first", each "additional" and each of the "n additional" switching group systems.

The statements in Box V are therefore based on the assumption that the phrase "said switching group system (1, 10.1, ..., 10.n)" in claims 1 and 2 is to be interpreted as follows: "wherein each of said switching group systems (1, 10.1, ..., 10.n) provided for each phase (R, S, T)".

Moreover, it is assumed that the phrase "wherein the or one of the intermediate switching group (7)" in claims 1

Box No. VIII Certain observations on the international application

and 2 is to be interpreted as follows: "wherein the or one of the intermediate switching groups (7)".